IN THE CLAIMS:

1. (Currently amended) For use in a wide-issue processor, a mechanism for identifying and tracking conditional instructions, comprising:

a conditional execution block state machine that tags and generates contemporaneous link pointers for instructions located in a conditional execution block, wherein said link pointers mark at least the beginning and end of a conditional execution block of instructions; and

conditional link pointer register sets, wherein each of said register sets corresponds to a single stage of a pipeline of said processor, that contain and cause said link pointers to move through each corresponding register of said register sets as said instructions associated with said link pointers and located in said conditional execution block move through each of said corresponding stages, said corresponding stages including a fetch/ decode stage and a group stage.

2. (Previously Presented) The mechanism as recited in Claim 1 further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said sets.

3. (Original) The mechanism as recited in Claim 2 wherein said conditional execution marking queue is a five-bit, six-entry queue and comprises a reordering multiplexer.

4. (Original) The mechanism as recited in Claim 1 further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions.

5. (Cancelled)

6. (Original) The mechanism as recited in Claim 4 further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register.

7. (Original) The mechanism as recited in Claim 6 wherein said conditional execution attribute queue is of variable depth and comprises a selecting multiplexer.

Claims 8-14 (Canceled)

15. (Currently amended) A wide-issue digital signal processor (DSP), comprising:

a pipeline having stages capable of executing instructions conditionally;

a wide-issue instruction issue unit;

a conditional execution block state machine, associated with said instruction issue unit, that tags and generates contemporaneous link pointers for instructions located in a conditional execution block, wherein said link pointers mark at least the beginning and end of a conditional execution block of instructions; and

conditional link pointer register sets, wherein each of said register sets corresponds to a single stage of a pipeline of said processor, that contain and cause said link pointers to move through each corresponding register of said register sets as said instructions associated with said link pointers and located in said conditional execution block move through each of said corresponding stages, said corresponding stages including a fetch/ decode stage and a group stage.

16. (Previously Presented) The DSP as recited in Claim 15 further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said sets.

17. (Original) The DSP as recited in Claim 16 wherein said conditional execution marking queue is a five-bit, six-entry queue and comprises a reordering multiplexer.

18. (Original) The DSP as recited in Claim 15 further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions.

19. (Canceled)

20. (Original) The DSP as recited in Claim 18 further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register.

21. (Original) The DSP as recited in Claim 20 wherein said conditional execution attribute queue is of variable depth and comprises a selecting multiplexer.

Claims 22-23 (Canceled)

24. (Previously Presented) The mechanism as recited in Claim 1, wherein:

said fetch/ decode stage is configured to:

fetch and decode instructions;

identify conditional execution instructions; and

generate said link pointers; and

said group stage is configured to:

check grouping and dependency rules;

group valid instructions;

execute return instructions; and

group conditional execution instructions and blocks.

Claim 25 (Canceled)

26. (Previously Presented) The DSP as recited in Claim 15, wherein:

said fetch/ decode stage is configured to:

fetch and decode instructions;

identify conditional execution instructions; and

generate said link pointers; and

said group stage is configured to:

check grouping and dependency rules;

group valid instructions;

execute return instructions; and

group conditional execution instructions and blocks.